



SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling

Stuart Sutherland, Simon Davidmann, Peter Flake

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In its updated second edition, this book has been extensively revised on a chapter by chapter basis. The book accurately reflects the syntax and semantic changes to the SystemVerilog language standard, making it an essential reference for systems professionals who need the latest version information. In addition, the second edition features a new chapter explaining the SystemVerilog "packages", a new appendix that summarizes the synthesis guidelines presented throughout the book, and all of the code examples have been updated to the final syntax and rerun using the latest version of the Synopsys, Mentor, and Cadance tools.

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