VHDL Coding Styles and Methodologies

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VHDL Coding Styles and Methodologies, Edition is a follow up book to the first edition of same book and to VHDL Answers to Frequently Asked Questions, first and second editions. This book was originally written as a teaching tool for a VHDL training course. The author began writing the book because he could not find a practical and easy to read book that gave in depth coverage of both, the language and coding methodologies. This edition provides practical information on reusable software methodologies for the design of bus functional models for testbenches. It also provides guidelines in the use of VHDL for synthesis. All VHDL code described in the book is on a companion CD. The CD also includes the GNU toolsuite with EMACS language sensitive editor (with VHDL, Verilog, and other language templates), and TSHELL tools that emulate a Unix shell. Model Technology graciously included a timed evaluation version of ModelSim, a recognized industry standard VHDL/Verilog compiler and simulator that supports easy viewing of the models under analysis, along with many debug features. In addition, Synplicity included a timed version of Synplify, a very efficient, user friendly and easy to use FPGA synthesis tool. Synplify provides a user both the RTL and gate level views of the synthesized model, and a performance report of the design. Optimization mechanisms are provided in the tool.

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